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a first semiconductor element formed in an element formation region defined by said partial-isolation insulating film in said semiconductor layer;
an interlayer insulting film formed on said first semiconductor element and said partial-isolation insulating film,
at least one of a power supply line and a ground line formed on said interlayer insulating film; and
a first complete-isolation insulating film formed throughout a portion directly below at least one of said power supply line and ground line.

REMARKS

Favorable reconsideration of this application, in view of the following comments and as presently amended, is respectfully requested.

Claim 1 is amended by the present response to correct for the minor informality noted on the top of page 2 of the Office Action.

Claims 1-20 are pending in this application. Claims 2-20 are withdrawn from consideration. Claim 1 was rejected under 35 U.S.C. §103(a) as unpatentable over U.S. patent 6,118,152 to Yamaguchi et al. (herein "Yamaguchi") In view of U.S. patent 5,747,846 to Iida et al. (herein "Iida").

Addressing the rejection to Claim 1, that rejection is traversed by the present response.

It is initially noted that Claim 1 is amended by the present response to clarify a feature recited therein. Specifically, Claim 1 now clarifies that the first complete-isolation insulating film is formed "throughout a portion directly below at least one of said power supply and

ground line". According to that feature, and with reference to Figure 2 in the present specification as a non-limiting example, the complete-isolation insulating film 23 is formed at a portion directly below the power supply line 21. In a further non-limiting embodiment shown, for example, in Figure 18 in the present specification, the first complete-isolation insulating film 51 is formed throughout a portion directly below a ground line 22.

The above-noted feature as clarified in Claim 1 distinguishes over the applied art.

The outstanding Office Action cites the teachings in Yamaguchi to meet the above-noted features in Claim 1. Specifically, the outstanding Office Action relies on Yamaguchi disclosing a first complete-isolation insulating film 6 and a ground line 19a in Figure 1. However, it is clear from Figure 1 in Yamaguchi that the insulating film 6 is *not formed* throughout a portion *directly* below the ground line 19a. It is clear from Figure 1 in Yamaguchi that polysilicone layer 7 is formed directly below the ground line 19a, and the insulating film 6 is *not formed directly below* the ground line 19a.

In such ways, the teachings in Yamaguchi do not meet the claim 1 features.

Further, no teachings in Iida can overcome the above-noted teachings in Yamaguchi.

Thereby, independent Claim 1 distinguishes over the applied art.

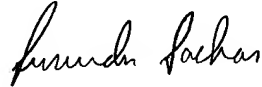
It is also noted that as each of Claims 2-7 depends on independent Claim 1, and thus independent Claim 1 is clearly generic to each of Claims 2-7. Therefore, each of Claims 2-7 must now be rejoined.

Thus, each of Claims 1-7 is in condition for allowance.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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IN THE CLAIMS

--1. (Twice Amended) A semiconductor device comprising:

an SOI substrate having a structure in which a semiconductor substrate, an insulating layer and a semiconductor layer are layered in this order;

a partial-isolation insulating film formed in a main surface of said semiconductor layer[:];

a first semiconductor element formed in an element formation region defined by said partial-isolation insulating film in said semiconductor layer;

an interlayer insulting film formed on said first semiconductor element and said partial-isolation insulating film;

at least one of a power supply line and a ground line formed on said interlayer insulating film; and

a first complete-isolation insulating film formed throughout a portion directly below at least one of said power supply line and ground line.--